

PATENT APPLICATION

Docket No.: D486

Inventor(s): Donald C. Mayer, Jon V. Osborn,
Ronald C. Lacoe & Everett E. King

Residence Addresses of the Inventors: Donald C. Mayer: 305
Via Colorin, Palos Verdes Estates, CA, 90274, Jon V. Osborn:
2371 Gillingham Circle, Thousand Oaks, CA, 91362, Ronald C.
Lacoe: 310 McKnight Road, Newbury Park, CA, 91320, and Everett
E. King: 12847 Winthrop Avenue, Granada Hills, CA, 91344, All
US Citizens.

Title: Annular Segment MOSFET

SPECIFICATION

Statement of Government Interest

The invention was made with Government support under
contract No. F04701-00-C-0009 by the Department of the Air
Force. The Government has certain rights in the invention.

Field of the Invention

The invention relates to the field of semiconductor
integrated circuits. More particularly, the invention relates
to semiconductor integrated circuit MOSFET devices having
annular topographi s.

Background of the Invention

The scaling of metal oxide silicon (MOS) integrated circuits has followed a relentless decrease in feature sizes with a corresponding increase in data throughput per chip for the past thirty years. However, the reduction in power supply voltages in each new generation has not scaled nearly as rapidly as the reduction in feature sizes of the MOS integrated circuits. This mismatch in downward scaling between feature sizes and applied voltages has resulted in substantial increases in electric fields in MOS integrated circuits, particularly in the channels and oxide layers of metal oxide silicon field effect transistors (MOSFETs).

Referring to Figure 1A, a prior art straight MOSFET is shown having uniform electric fields extending across the gate from the source to the drain. There is an insulating oxide layer between the gate and the channel region in the silicon. As the dimensions of the straight MOSFET decrease, the strength of the electric fields increases, for a given applied voltage. In a conventional MOSFET, current is carried by inversion layer electrons moving under the influence of the lateral electric field in the channel. The channel has two opposing ends that are parallel to each other. The lateral electric field in the MOSFET channel that causes the transistor current to flow varies monotonically from the source, where the field is low, to the drain, where the field peaks sharply. The high field at the drain is well known to cause damage to the MOSFET as

1 carriers are accelerated by the high electric field and some
2 carriers are disadvantageously scattered into the gate oxide
3 leading to damage and poor reliability. This damage limits the
4 current capacity of the MOSFET, and will eventually lead to
5 failure of the MOSFET. The conventional use of lightly doped
6 drains in MOSFET channels has reduced the channel electric
7 fields. However, as the dimensions of the MOSFET features
8 continue to shrink in size, the electric fields will continue
9 to correspondingly increase.

10
11 Referring to Figure 1B, an experimental circular MOSFET
12 has a gate that is curved and extends between the source and
13 drain. The circular MOSFET has a gate structure in the shape of
14 a circle. With a source in the center of the circular gate and
15 a drain on the outside of the circular gate, the electric
16 fields can diverge across the gate from the source to the drain
17 so as to decrease the electric field at the edge of the drain.
18 When the drain is in the center of the circular gate and the
19 source is outside the circular gate, the electric fields into
20 the drain would converge disadvantageously producing an
21 increasing electric field at the edge of the drain. A circular
22 MOSFET has a gate that has no ends, and the circular gate is
23 continuous. A circular MOSFET disadvantageously uses a
24 relatively large amount of silicon square area, relative to the
25 gate size. A conventional serpentine MOSFET, not shown, has a
26 gate with semicircle-curved portions. The serpentine MOSFET
27 structure has one hundred and eighty degree bends that are
28 alternating inflection curve structures. That is, the

1 serpentine MOSFETs have a plurality of one hundred and eighty
2 d gree curved bends. Th gate is curved one way, and then
3 curved the other way. At each point of curvature change is a
4 curve inflection point. Hence, the serpentine MOSFET has a
5 plurality of curve inflections along the length of the gate.
6 The serpentine MOSFET has a gate and a channel that has two
7 opposing channel ends that are parallel to each other. The
8 channel ends of the gates are defined by two opposing locations
9 under the gate where the underlying channel silicon ends. The
10 semicircle MOSFET has a gate that has two opposing channel ends
11 that are in alignment as well as being parallel to each other.
12 The semicircle MOSFET has a gate and channel in the shape of a
13 horseshoe. The serpentine MOSFET would have both converging and
14 diverging electric fields across the gate at respectively
15 alternating curved-gate portions. As such, the serpentine
16 MOSFET has alternating gate-inflecting portions providing both
17 diverging and converging electric fields. The converging
18 electric field lines disadvantageously provide high electric
19 fields into the drain in the alternating portions of the gate.
20 The semicircle and serpentine MOSFET also disadvantageously
21 require a large relative square area of silicon. These and
22 other disadvantages are solved or reduced using the invention.

23
24
25
26
27
28 ///

Summary of the Invention

An object of the invention is to provide an annular segment MOSFET structure.

Another object of the invention is to provide an annular segment MOSFET structure having diverging electric field lines between the source and drain of the MOSFET.

Yet another object of the invention is to provide an annular segment MOSFET structure having diverging electric field lines between the source and drain of the MOSFET for reducing the energy of hot carriers injected into the gate insulating oxide layer over the channel.

Still another object of the invention is to provide an annular segment MOSFET structure with a curved gate having diverging electric field lines between the source and drain of the MOSFET for reducing the energy of hot carriers injected into the oxide layer for improved reliability of the MOSFET.

Yet a further object of the invention is to provide an annular segment MOSFET structure with a curved gate having an arc length less than a semicircle and having diverging electric field lines between the source and drain of the MOSFET for reducing the energy of hot carriers injected into the oxide layer for improved reliability of the MOSFET.

1 Yet a further object of the invention is to provide an
2 annular segment MOSFET structure with a curved gate having an
3 arc length less than a semicircle and having diverging electric
4 field lines between the source and drain of the MOSFET for
5 reducing the energy of hot carriers injected into the oxide
6 layer for improved reliability of the MOSFET and for providing
7 high density integration of MOSFETs on a square area of
8 silicon.

9
10 The present invention is directed to improving the
11 reliability of MOSFETs while enabling high-density integration
12 of the MOSFETs through the use of annular segment curved gates.
13 An annular segment MOSFET has a curved gate so as to improve
14 reliability of the MOSFET by reducing the electric field
15 strength between the source and drain and into the drain of the
16 MOSFET while enabling a high integration density. Discovery is
17 made that diverging electric fields into the drain of MOSFETs
18 tends to lower the high energy of the hot carriers that are
19 injected into the drain so as to lead to a significant
20 improvement of the reliability of the MOSFET. With lower
21 electric fields, the velocity of the hot carriers into the
22 drain is decreased with decreased energy leading to less damage
23 of the oxide layer with a corresponding improvement in
24 reliability. By sufficiently diverging the electric fields
25 through the use of the annular segment gate structure, the
26 electric fields diverge into the drain with a corresponding
27 reduction in the electric field strength so as to reduce the
28 energy of the hot carriers injected into the drain so as to

1 minimize damage of the oxide layer for improved reliability and
2 extended operational life of the MOSFET. The annular segment
3 structure provides improv d reliability while preserving a high
4 integration density.

5
6 In the general form of the invention, the gate is curved
7 without an opposing curve inflection and the arc length of the
8 curved gate is less than a circle, and preferably less than a
9 semicircle. In the preferred form, a quarter-circle annular
10 segment structure and eighth-circle annular segment structure
11 are used to enable both improved reliability while preserving
12 the high integration density of conventional straight MOSFET
13 structures. These and other advantages will become more
14 apparent from the following detailed description of the
15 preferred embodiment.

16
17
18
19
20
21
22
23
24
25
26
27
28 ///

Brief Description of the Drawings

Figure 1A depicts a prior art straight N-channel MOSFET.

Figure 1B is depicts a prior art circular N-channel MOSFET.

Figure 2A depicts a quarter-circle annular N-channel MOSFET.

Figure 2B depicts an eighth-circle annular N-channel MOSFET.

///

Detailed Description of the Preferred Embodiment

An embodiment of the invention is described with reference to the figures using reference designations as shown in the figures. Referring to Figures 2A and 2B, a quarter circle annular segment metal oxide silicon field effect transistor (MOSFET) is shown, and an eighth circle annular segment MOSFET is shown, respectively. These two preferred annular segment MOSFETs are generally characterized as having a curved noninflecting gate structure that is curved to be less than a semicircle. A source connector is a conductive interconnect, preferably made of a metal such as aluminum, tungsten, or titanium, and having a source contact that makes contact with and is disposed over n-type silicon. A gate is a conductive material disposed over a channel region of the n-type silicon. Between the gate and the channel region of the n-type silicon is disposed an oxide layer, as is conventional practice. A drain connector is a conductive interconnect preferably having a plurality of drain contacts that make contact with and are disposed over the n-type silicon. Between the gate channel under the gate and the source contact is a source made of n-type silicon. Between the gate channel under the gate and the drain contacts is a drain made of n-type silicon. The source and drain are portions of n-type silicon that are isolated by a surrounding p-type silicon well. The gate extends over the p-type silicon. The channel is formed by inversion of the silicon under the gate from p-type to n-type by an applied gate voltage. The gate extends slightly beyond the source and drain

1 edges for reducing edge affects. The channel ends of the gate
2 are defined by extension of the source and drain edges under
3 the gate. In operation, a voltage potential is applied between
4 the source connector and the drain connector so as to establish
5 the electric field extending between the source and the drain.
6 Conduction of current between the source and drain through the
7 channel is controlled by a gate voltage applied to the gate.

8
9 The quarter circle gate shown in Figure 2A has a
10 noninflecting curve shape that preferably forms a ninety-degree
11 arc for forming a quarter circle annular segment MOSFET. The
12 eighth circle gate shown in Figure 2B has a noninflecting curve
13 shape that preferably forms a forty-five degree arc for forming
14 an eighth circle annular segment MOSFET. Because the gate is
15 made of a noninflecting curved structure partially
16 circumscribing the source, a source radial distance from source
17 contact to the inside edge of gate where the source abuts the
18 gate channel is less than a drain radial distance from the
19 source contact to the outside edge of the gate where the gate
20 channel silicon abuts the drain silicon. That is, the source
21 radial distance is less than the drain radial distance, which
22 produces a diverging electric field effect. As such, electric
23 field lines extending between the source and the drain diverge
24 thereby reducing the electric field intensity at the drain. The
25 reduction of the electric field serves to reduce the energy of
26 the hot carriers so as to reduce hot carrier damage of the
27 insulating oxide layer between the gate and channel region. The
28 ends of the gate extending over the p-type well produce edge

1 effects that insignificantly distort the uniformly diverging
2 electric fields extending from the source to the drain.
3 However, gate edges do modestly reduce radiation immunity of
4 these annular segment MOSFETs. Because the preferred arc length
5 is substantially less than a complete semicircle, the MOSFET
6 device can be aligned during processing for maximum integration
7 density. Particularly, the gate is curved without an opposing
8 inflection curvature portion.

9
10 Significantly, in this compact annular segment MOSFET
11 structure, the two opposing ends of the noninflecting-curved
12 gate are neither in alignment with each other nor parallel to
13 each other. The gate is disposed over the channel. One end of
14 the gate with an edge extends slightly over the p-type silicon
15 well. On the opposing end of the gate, the gate extends over
16 the p-type well to make an external connection to a gate
17 control voltage. The channel ends of the gate are defined by
18 the underlying channel where the n-type silicon channel ends.
19 The curved gate and corresponding channel between these two
20 opposing channel ends are curved and noninflecting. These
21 channel ends are at differing relative angles. In the case of
22 the quarter circle annular segment MOSFET, the channel ends are
23 at ninety degrees relative to each other and are thus neither
24 parallel to each other, nor in alignment to each other. In the
25 case of the eighth circle annular segment MOSFET, the channel
26 ends are at forty-five degrees relative to each other and are
27 thus neither parallel to each other, nor in alignment to each
28

1 other. In both cases, the channel is defined by a noninflecting
2 curve extending between nonparallel nonaligned channel ends.

3
4 Similar p-type MOSFETs can be likewise constructed with an
5 inner electrode, a curved gate, and an outer electrode. In the
6 preferred form of p-type MOSFETs, the inner electrode is the
7 source and the outer electrode is the drain. The electric field
8 lines are spread out, that is, diverge, as the electric field
9 extends towards the outer electrode for reducing the drain
10 electric field for the same applied voltage and channel length.
11 When the outer electrode is selected as the drain in a p-type
12 silicon MOSFET, and the inner electrode is selected as the
13 source, the electric fields at the drain likewise are reduced
14 for reducing hot-carrier energy.

15
16 It should now be apparent that diverging electric field
17 strength is realized by forming a noninflecting-curved gate
18 between an inner electrode and an outer electrode. While the
19 preferred form uses a noninflecting curved structure that is a
20 portion of the circle, other noninflecting curved structures,
21 such as a portion of an ellipse or parabola or other curved
22 structures, can be used so long as curved structure is
23 noninflecting so as to diverge the electric field extending
24 between the source and drain. The diverging electric field
25 reduces hot carrier energy for reducing hot carrier damage of
26 the oxide between the gate and channel. In the preferred form,
27 n-type silicon is used for forming an inner source electrode
28 and an outer drain electrode. The preferred form provides

1 improved reliability of the MOSFET while pr serving high
2 integration densities. The MOSFET can be made of differing
3 materials, but is preferably made using conventional MOS
4 processes and mat rials. Those skilled in the art can make
5 enhancements, improvements, and modifications to the invention,
6 and these enhancements, improvements, and modifications may
7 nonetheless fall within the spirit and scope of the following
8 claims.

9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28 ///